Attorney Docket No. 109263-132220 PATENT
IPN: P16322

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Application of:	Examiner: Kiesha L. Rose
Cynthia H. Polsky et al.	Art Unit: 2822
Application No.: 10/698,837	Confirmation No.: 1277
Filed: October 31, 2003	**CERTIFICATE OF TRANSMISSION/MAILING**
For: Redistribution of Substrate Interconnects	I hereby certify that this correspondence is being facsimile transmitted to the USPTO, electronically transmitted to the USPTO, or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450 on the date shown below:
	Typed or Printed: Heather L. Adamson
	Signature: /Heather L. Adamson/ Date: 09/13/2006

Mail Stop Appeal Brief-Patents
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

APPELLANT'S BRIEF IN SUPPORT OF APPELLANT'S APPEAL TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

To the Honorable Commissioner for Patents:

This brief is in support of a Notice of Appeal to the Board of Patent Appeals and Interferences filed on August 7, 2006, appealing the decision of the Examiner in the Advisory Action mailed July 7, 2006, maintaining the rejections of all pending claims of the above-captioned application as set forth in the Final Office Action mailed April 10, 2005 ("Final Office Action").

Appellant respectfully requests consideration of this appeal by the Board of Patent Appeals and Interferences for allowance of the present patent application.

I. REAL PARTY IN INTEREST

The real party in interest in the above-identified application is Intel Corporation, 2200 Mission College Blvd., Santa Clara, CA 95052.

II. RELATED APPEALS

The Appellant's undersigned attorney and the assignee identified above are not aware of other appeals or interferences that would directly affect or be directly affected by, or have a bearing on the Board's decision in the subject appeal.

III. STATUS OF THE CLAIMS

Claims 6-9, 11, and 12 stand rejected as failing to comply with the written description requirement of 35 U.S.C. § 112, ¶ 1.

Claim 6-9, 12, and 26-29 stand rejected under § 102(b) as being anticipated by U.S. Publication 2002/0117330 of Eldridge et al. ("*Eldridge*").

Claim 11 stands rejected under § 103(a) as being obvious in view of *Eldridge*.

Appellant appeals all claim rejections.

IV. STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Final Office Action.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Independent claims 6, 26, and 28 are directed to various embodiments of a semiconductor device. Independent claim 6 is directed to a semiconductor device comprising a carrier substrate having a bond pad (Spec. ¶ [0046], lines 4-5, with reference to elements 5, 61, and 63 of Fig. 6), and a first microelectronic die substrate (Spec. ¶ [0028], lines 1-4, with reference to element 1 of Fig. 1) including an active side (Spec. ¶ [0029], lines 6-7, with reference to element 12 of Fig. 1), a back side (Spec. ¶ [0031], lines 2-5, with reference to element 30 of Fig. 1), an active side interconnect disposed on the active side and coupled to the bond pad of the carrier substrate (Spec. ¶ [0029], lines 1-2 and 6-9, with reference to element 20 of Fig. 1;Spec. ¶ [0046], lines 4-7, with reference to element 20 of Fig. 6), a backside interconnect disposed on the back side and coupled to and in substantial vertical alignment with the active side interconnect (Spec. ¶ [0031], lines 2-5, with reference to element 36 of Fig. 1; *see also* element 36 of Fig. 6) and a redistributed interconnect of the backside interconnect disposed on the backside and coupled to and offset from the backside interconnect (Spec. ¶ [0039], lines 5-8, with reference to element 50 of Fig. 4; *see also* element 50 of Fig. 6). The semiconductor device of claim 6 further comprises an interconnect material comprising a conductive material without a wire stem (Spec. ¶¶ [0040]- [0045], generally, with reference to element 54 of Fig. 5; *see also* element 54 of Fig. 6), the interconnect material being coupled directly with the redistributed interconnect (Spec. ¶ [0046], lines 13-16, with reference to Fig. 6); and an interconnect of a second microelectronic die substrate electrically and directly coupled to the interconnect material (Spec. ¶ [0046], lines 13-16, with reference to element 21 of Fig. 6).

Independent claim 26 contains most of the same elements of claim 6 that will not be repeated. The difference between claim 6 and 26 lies in the interconnect material. Claim 26 comprises an interconnect material consisting of an electrically conductive reflowable material (Spec. ¶ [0040], lines 3-5, with reference to element 54 of Fig. 5; Spec. [0042], lines 8-10; Spec. [0043], lines 10-13; Spec. [0046], lines 5-7 and 14-16, with reference to element 54 of Fig. 6), the interconnect material being coupled directly with the redistributed interconnect (Spec. ¶ [0046], lines 13-16, with reference to Fig. 6).

Independent claim 28 contains most of the same elements of claims 6 and 26 that will not be repeated. The difference between claims 6 and 26, and 28 lies in the interconnect material. Claim 28 comprises an interconnect material consisting of an electrically conductive adhesive (Spec. ¶ [0040], lines 3-5; Spec. [0041], lines 2-4; Spec. [0045], lines 1-6), the interconnect material being coupled directly with the redistributed interconnect (Spec. ¶ [0046], lines 13-16, with reference to Fig. 6).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. The specification is objected to for introducing new matter into the disclosure, in violation of 35 U.S.C. § 132(a) due to the inclusion of the limitation "without a wire stem."

B. Claims 6-9, 11, and 12 stand rejected for failing to comply with the written description requirement of 35 U.S.C. § 112, ¶ 1 due to the inclusion of the limitation "without a wire stem."

C. Claims 6-9, 12, and 26-29 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Publication 2002/0117330 of Eldridge et al. ("*Eldridge*").

D. Claim 11 stands rejected under 35 U.S.C. § 103(a) as being obvious in view of *Eldridge*.

VII. ARGUMENT

A. Objection to the inclusion of the language "without a wire stem" in the specification under 35 U.S.C. § 132(a) is improper because the language is supported by the original disclosure and thus is not new matter.

The January 13, 2006 amendment to the specification, in response to the October 19, 2005 Office Action, was objected to under 35 U.S.C. § 132(a) as introducing new matter into the disclosure. Specifically, it was asserted that the inclusion of the phrase "without a wire stem" into the specification introduced new matter not supported by the original disclosure. Appellant respectfully disagrees.

Section 132(a) prohibits the introduction of new matter into the disclosure. 35 U.S.C. § 132(a). However, "information contained in any one of the specification, claims or drawings of the application as filed may be added to any other part of the application without introducing new matter." M.P.E.P. § 2163.06 (8th ed., rev. 3., Aug. 2005) (emphasis added). The fundamental inquiry is whether the information added by amendment is contained, explicitly or implicitly, in the original application. *Schering Corp. v. Amgen Inc.*, 222 F.3d 1347, 1352, 55 U.S.P.Q.2d 1650, 1653 (Fed. Cir. 2000) (citing *Litton Sys., Inc. v. Whirlpool Corp.*, 728 F.2d 1423, 1438, 221 U.S.P.Q. 97, 106 (Fed. Cir. 1984)).

In the subject patent application, support for an interconnect material "without a wire stem" is found in the specification and the drawings. The Background section of the specification explicitly describes the undesirability of wire stems. For example, it states:

> The land pads on the die were traditionally located on the active side about the peripheral edge of the substrate. The corresponding carrier

> substrate bond pads were located such that they would encircle the die when the die backside was adhesively bonded to the carrier substrate. Interconnection was made by welding wire between the land pads and the bond pads. Such wires, commonly made of gold, have been referred to as bond wires, and the process referred to as wire bonding. This type of interconnection occupies an unacceptably large portion of the carrier substrate.

Spec. ¶ [0005] (emphasis added). The specification continues:

> The trend for higher density packaging has lead to the concept of stacking one die on top of another die in a vertical orientation. The land pads of a first die are interconnected with bond pads on the carrier substrate using an appropriate process, such as, but not limited to, a conventional controlled collapse chip connection (C4) reflow process, compression bonding, ultrasonic bonding, and conductive adhesive. A second die backside of a second die is coupled to a first die backside of the first die, such as by using adhesive. The interconnects of the second die are interconnected with interconnects on the carrier substrate using wire-bonding. Though, this process provides a stacked configuration for the two die, carrier substrate surface area is still taken up by the bond pads that are wire-bonded to the second die. This process produces a package with undesirable form factor and inherent fragility of the wire-bonds which effects product reliability.

Spec. ¶ [0009] (emphasis added). Thus, the original specification clearly identifies prior art packages enlisting wire bonds (i.e., wire stems) as being undesirable because of the space consumption and fragility of the wire-bonding.

Furthermore, throughout the remainder of the original specification, detailed descriptions are set forth for forming a die with a redistribution layer and interconnecting the die with a carrier substrate and another die. Nowhere is it disclosed, whether explicit or implicit, that wire stems form any part of the interconnection. The original specification discloses an interconnect material 54 and the processes for forming and

depositing the interconnect material 54. Spec., ¶¶ [0040]-[0045]. For example, the original specification discloses the following:

- "Interconnect material 54 is passed through apertures in the screen [in a screen printing process] and onto the lateral interconnect 50. A reflow process is used to soften or melt the interconnect material 54 to form rounded interconnects . . ." Spec. ¶ [0042], lines 7-10 (emphasis added).

- "A reflow process may be used to soften or melt the interconnect material 54 to form spherical interconnects, due to surface tension of the molten interconnect material 54 . . ." Spec. ¶ [0043], lines 10-13 (emphasis added).

- "During a reflow process, the interconnect material 54 melts and forms a unitary electrical interconnection between second die interconnect 21 and the lateral interconnect 50." Spec. ¶ [0046], lines 14-16 (emphasis added).

Such processes indicate that the interconnect material cannot include a wire stem. For instance, screen printing of the disclosed interconnect material is a clear indication that wire stems necessarily are absent. It would be difficult, if not impossible, to pass the interconnect material through apertures of a screen and form rounded interconnects if a wire stem were present in the interconnect material. Most certainly, if wire stems were even a possible embodiment of the disclosed interconnection, such information necessarily would have been set forth explicitly, particularly given the shortcomings of wire stems as discussed in the Background section of the original specification. At a minimum, the specification implicitly discloses that the interconnect material cannot include a wire stem.

Bolstering the assertion that the interconnection as taught by the original specification necessarily requires the omission of any wire stems are the original

drawings. The original drawings clearly illustrate a die including interconnect material "without a wire stem." Specifically, Figures 5 and 6 of the original disclosure shows an interconnect material 54, neither of the drawings including any semblance of a wire stem, whether explicit or implicit.

Taken with the language explicitly denigrating wire-bonding, a reading of the remaining portion of the original specification as well as the drawings leads the reader, whether of ordinary skill in the art or not, to one simple conclusion: the disclosure at least implicitly teaches an alternative solution to those substrate interconnections enlisting inferior wire stems.

Therefore, inclusion of the language "without wire stems" in the specification does not constitute new matter under 35 U.S.C. § 132 because such was disclosed in the original specification and drawings, and accordingly, Appellant respectfully requests withdrawal of the requirement to cancel said language therefrom.

B. Rejection of claims 6-9, 11, 12, and 26-29 under 35 U.S.C. § 112, ¶ 1 is improper because the limitation "without a wire stem" is supported by the original disclosure.

The September 27, 2005 amendments to the claims submitted in response to the July 27, 2005 Office Action were rejected under 35 U.S.C. § 112 as failing to comply with the written description requirement. Specifically, it was asserted that the inclusion of the phrase "without a wire stem" in the claims introduced subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the Appellant, at the time the application was filed, had possession of the claimed invention.

Section 112 requires: "a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art . . . to make and use the same." 35 U.S.C. § 112. Essentially, to satisfy the § 112 requirement, a patent specification must describe the claimed invention with sufficient detail to allow a person of ordinary skill in the art to conclude that the inventor had possession of the claimed invention. *Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1562-63, 19 U.S.P.Q.2d 1111, 1115-16 (Fed. Cir. 1991).

It is well-settled that the written description is not limited to the words of the specification; rather, an applicant shows possession of the claimed invention by describing the claimed invention with all of its limitations using such descriptive means as words and drawings that fully set forth the claimed invention. See, e.g., *Vas-Cath Inc.*, 935 F.2d at 1564 ("drawings alone may be sufficient to provide the 'written description of the invention' required by § 112, first paragraph"). The test is simply whether the written description, taken as a whole, discloses the claimed invention, not

whether it expressly discloses it: "newly added claim limitations [may] be supported in the specification through express, implicit, or inherent disclosure." M.P.E.P. § 2163 (emphasis added); see also *In re Herschler*, 591 F.2d 693, 701, 200 U.S.P.Q. 711, 717 (C.C.P.A. 1979) ("It is not necessary that the application describe the claim limitations exactly, but only so clearly that one having ordinary skill in the pertinent art would recognize from the disclosure that appellants invented processes including those limitations").

In this case, and as discussed previously, the written description, when taken as a whole, discloses the claimed invention. The words and the drawings of the disclosure, including the Background and Detailed Description sections as well as the drawings, leads the reader to the inevitable conclusion that the disclosure teaches an alternative solution to substrate interconnection, one not enlisting inferior wire stems. Specifically, the words of the specification explicitly denigrate wire-bonding and teach interconnection via methods not conducive to wire stems, and the drawings show interconnection without wire stems. Even if one were to argue that the original specification did not expressly state that the interconnect material does not have wire stems, such a teaching nevertheless is supported by the original specification and the drawings at least implicitly.

Therefore, inclusion of the language "without wire stems" in the claims complies with the written description requirement of 35 U.S.C. § 112 because one skilled in the art would have concluded that the Appellant had possession of the claimed invention. Accordingly, Appellant respectfully requests withdrawal of the rejections of claims 6-9 and 11-12 under 35 U.S.C. § 112.

C. Rejection of claims 6-9, 12, and 26-29 under 35 U.S.C. § 102(b) is improper because Eldridge fails to teach each and every limitation of the claims.

Claims 6-9, 12, and 26-29 stand rejected under 35 U.S.C. § 102(b) as being anticipated by *Eldridge*. Appellant respectfully asserts that said claims are allowable over *Eldridge* because *Eldridge* fails to teach each and every limitation of said claims.

It is well settled that anticipation under 35 U.S.C. § 102 requires the clear and unambiguous disclosure in a single piece of prior art of each and every limitation of a claimed invention. *Electro Med. Sys. S.A. v. Cooper Life Sciences*, 34 F.3d 1048, 1052, 32 U.S.P.Q.2d 1017, 1019 (Fed. Cir. 1994). Thus, to anticipate the present invention, *Eldridge* must clearly and unambiguously disclose every element of claims 6-9, 12, and 26-29.

Claim 6 includes, among other things, "an interconnect material comprising a conductive material without a wire stem, the interconnect material being coupled directly with the redistributed interconnect; and an interconnect of a second microelectronic die substrate electrically and directly coupled to the interconnect material." (emphasis added). Appellant submits that such a structure is not disclosed in *Eldridge.* That is, Appellant submits that when all limitations, including the limitation "without a wire stem," are given their full weight, claim 6 is allowable over *Eldridge*.

The Final Office Action states that Figures 32 and 35 of Eldridge show each of the limitations of claim 6. Figure 32 is cited for allegedly showing a microelectronic die substrate (3208) and Figure 35 for allegedly disclosing the contact areas or structures (i.e., redistributed interconnect) as recited in original claim 6. However, neither Figure 32 nor 35, each taken alone or in combination, shows "an interconnect material

comprising a conductive material without a wire stem, coupled directly with the redistributed interconnect; and an interconnect of a second microelectronic die substrate electrically coupled directly to the interconnect material." At best, *Eldridge* only discloses in Figure 35 a first printed circuit board (PCB) 3550 having a plurality of via holes coupled to contact areas (i.e., redistributed interconnects) disposed on a surface of the first PCB 3550, the contact areas being coupled to bump-like contact structures (i.e., interconnect material) 3568 with wire stems that are indirectly coupled to the contact pads (i.e., interconnects) 3521-3526 of a second PCB 3520 through resilient contact structures (i.e., wire stems) 3561-3566 and interposer substrate 3560. Thus, *Eldridge* does not disclose "a conductive interconnect material without a wire stem coupled directly with the redistributed interconnect; and an interconnect of a second microelectronic die substrate electrically coupled directly to the interconnect material."

Appellant further respectfully disagrees with the assertion in the Office Action that *Eldridge* anticipates claim 6 based on the combination of different elements shown separately in Figures 32 and 35 of *Eldridge*. In particular, the Examiner appears to have selectively pasted together different elements from Figures 32 and 35 in order to come up with the claimed invention as recited in claim 6 even though there appears to be no basis or nexus for doing so. That is, *Eldridge* appears to stand for the proposition that spring-like wire stems coated with overcoat material can be used in interconnecting different electronic components. Figures 32 and 35 simply show how such spring-like wire stems can be used in two different scenarios. The Examiner appears to have cited Figure 32 for the proposition that it shows a microelectronic die substrate while Figure 35 was cited for the proposition that it shows offset contact areas, which in Figure 35,

are disposed on a PCB. Appellant submits that there is no motivation or suggestion in either the drawings (Figures 32 or 35) themselves or in the specification of *Eldridge* for combining the microelectronic die substrate of Figure 32 with the offset contact areas of Figure 35, as recited in claim 6. Therefore, for at least the above stated reasons, claim 6 is allowable over *Eldridge*.

Claims 7-9 and 12 each depend upon independent claim 6 incorporating their corresponding limitations. Thus, for at least the above stated reasons, claims 7-9 and 12 are allowable over *Eldridge*.

Independent claims 26 and 28 recite features similar to those of claim 6 except that they do not include the phrase "without a wire stem." Instead, claims 26 and 28 recite the features "an interconnect material consisting an electrically conductive reflowable material" and "an interconnect material consisting an electrically conductive adhesive," respectively. Such features are not taught by *Eldridge*. Appellant therefore respectfully submits that claims 26 and 28 are allowable over *Eldridge*. Claims 27 and 29 depend from independent claims 26 and 28, incorporating their features. Thus, for at least the same reason that claims 26 and 28 are patentable, claims 27 and 29 likewise are patentable.

D. Rejection of claim 11 under 35 U.S.C. § 103(a) is improper because Eldridge fails to teach each and every limitation of the claim.

Claim 11 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over *Eldridge*. In particular, it appears that the Examiner is rejecting claim 11 based on the fact that claim 11 recites a "product by process" limitation and that since the Examiner rejected claim 6, which claim 11 depends from, that claim 11 is

likewise unpatentable over *Eldridge*. However and as previously stated, Appellant submits that claim 6 is patentable over *Eldridge*, and because of its dependency to claim 6, claim 11 is likewise patentable over *Eldridge* under 35 U.S.C. § 103(a).

VIII. CONCLUSION

Appellant respectfully submits that all the appealed claims in this application are patentable and requests that the Board of Patent Appeals and Interferences overrule the Examiner and direct allowance of the rejected claims.

This brief is submitted in triplicate, along with a check for $500 to cover the appeal fee for one other than a small entity as specified in 37 C.F.R. § 1.17(c). It is not believed that any fees, including extension of time fees, are needed. However, should additional fees be necessary, please charge Deposit Account No. 500393. In addition, please credit any overages to the same account.

Respectfully submitted,
SCHWABE, WILLIAMSON & WYATT, P.C.

Dated: 09/13/2006

/Angela M. Sagalewicz/
Angela M. Sagalewicz
Registration No. 56,113

Pacwest Center, Suite 1900
1211 SW Fifth Avenue
Portland, Oregon 97204
Telephone: 503-222-9981

CLAIMS APPENDIX

1. (Cancelled)

2. (Cancelled)

3. (Cancelled)

4. (Cancelled)

5. (Cancelled)

6. (Previously presented) A semiconductor device, comprising:

a carrier substrate having a bond pad;

a first microelectronic die substrate, the first microelectronic die substrate including,

an active side and a back side,

an active side interconnect, the active side interconnect disposed on the active side, coupled to the bond pad of the carrier substrate,

a backside interconnect disposed on the back side, coupled to and in substantial vertical alignment with the active side interconnect,

a redistributed interconnect of the backside interconnect, disposed on the backside, coupled to and offset from the backside interconnect;

an interconnect material comprising a conductive material without a wire stem, the interconnect material being coupled directly with the redistributed interconnect; and

an interconnect of a second microelectronic die substrate electrically and directly coupled to the interconnect material.

7. (Original) The semiconductor device of claim 6, wherein the first substrate comprises:

a metal layer having a first side and a second side;

a first dielectric layer adjacent to the first side of the metal layer;

a first aperture in the first dielectric layer, the first aperture exposing a portion of the first side of the metal layer to define the active side interconnect;

a second dielectric layer adjacent to the second side of the metal layer; and

a via extending from the backside interconnect through the second dielectric layer to the second side of the metal layer to electrically couple the backside interconnect to the metal layer.

8. (Original) The semiconductor device of Claim 6, wherein the redistributed interconnect comprises:

a conductive trace coupled to and extending from the backside interconnect to a selected location;

a third dielectric layer overlaying the conductive trace; and

an aperture in the third dielectric layer at the selected location.

9. (Previously presented) The semiconductor device of Claim 8, wherein the selected location for the redistributed interconnect corresponds to the interconnect of the second microelectronic die substrate.

10. (Cancelled)

11. (Previously presented) The semiconductor device of claim 6, wherein the second microelectronic die substrate is coupled to the redistributed interconnect by a process selected from the group consisting of reflow bonding, thermal compression bonding, and ultrasonic bonding.

12. (Original) The semiconductor device of Claim 6, wherein the redistributed interconnect is not in vertical alignment with the backside interconnect.

13. (Withdrawn) A method comprising:

providing an active side interconnect to an active side of a substrate;

providing a backside interconnect to a back side of the substrate with the backside interconnect being coupled to and in substantial vertical alignment with the active side interconnect; and

providing a redistributed interconnect of the backside interconnect on the backside, the redistributed interconnect being coupled to and offset from the backside interconnect.

14. (Withdrawn) The method of Claim 13, wherein providing the redistributed interconnect comprises:

depositing a conductive trace on the back side;

coupling the conductive trace to the backside interconnect;

extending the conductive trace to a selected location;

placing a third dielectric layer over the conductive trace; and

forming an aperture in the third dielectric layer at the selected location.

15. (Withdrawn) The method of Claim 13, wherein providing the backside interconnect comprises forming a via that extends from the backside interconnect through a second dielectric layer to a metal layer and filling the via with an electrically conductive material.

16. (Withdrawn) The method of claim 13, further comprising;

providing a carrier substrate having a bond pad

providing a second substrate having an interconnect;

coupling the active side interconnect to the carrier substrate bond pad; and

coupling the interconnect of the second substrate to the redistributed interconnect.

17. (Withdrawn) The method of Claim 16, wherein coupling the interconnect of the second substrate to the redistributed interconnect is performed by a process selected from the group including reflow bonding, thermal compression bonding or ultrasonic bonding.

18. (Withdrawn) A method for redistributing interconnects, comprising:

providing a substrate having an active side and a backside, the active side having an active side interconnect;

forming a via in the backside extending from a surface of the backside to a metal layer within the substrate;

filling the via with an electrically conductive material such that a backside interconnect is formed at or substantially near the surface of the backside and in electrical communication with the metal layer;

depositing a conductive trace on the backside surface such that the conductive trace extends from the backside interconnect to a selected location on the back side surface;

depositing a dielectric layer on the back side surface such that it overlays the conductive trace; and

defining a redistributed interconnect of the backside interconnect at the selected location.

19. (Withdrawn) The method of Claim 18, wherein defining the redistributed interconnect comprises forming an aperture in the dielectric layer at the selected location to expose a portion of the conductive trace.

20. (Withdrawn) The method of Claim 19, wherein forming the aperture comprises etching a portion of the dielectric layer at the selected location to expose a portion of the conductive trace.

21. (Withdrawn) The method of Claim 18, further comprising choosing the selected location to correspond to a location of a complementary interconnect of a substrate in facing relationship there with.

22. (Withdrawn) The method of Claim 18, wherein depositing the conductive trace comprises forming a patterned electrically conductive layer on the backside surface using a photolithography process.

23. (Withdrawn) The method of Claim 18, further comprising depositing a conductive interconnect material into the dielectric aperture such that the conductive interconnect material is coupled to the redistributed interconnect and extends above the dielectric layer.

24. (Withdrawn) The method of claim 18, further comprising;

providing a carrier substrate having a bond pad;

providing a second substrate having an interconnect;

coupling the active side interconnect to the carrier substrate bond pad; and

coupling the interconnect of the second substrate to the redistributed interconnect.

25. (Withdrawn) The method of Claim 24, wherein coupling the interconnect of the second substrate to the redistributed interconnect is performed by a process selected from the group including reflow bonding, thermal compression bonding or ultrasonic bonding.

26. (Previously presented) A semiconductor device, comprising:

a carrier substrate having a bond pad;

a first microelectronic die substrate, the first microelectronic die substrate including,

an active side and a back side,

an active side interconnect, the active side interconnect disposed on the active side, coupled to the bond pad of the carrier substrate,

a backside interconnect disposed on the back side, coupled to and in substantial vertical alignment with the active side interconnect,

a redistributed interconnect of the backside interconnect, disposed on the backside, coupled to and offset from the backside interconnect;

an interconnect material consisting an electrically conductive reflowable material, the interconnect material being coupled directly with the redistributed interconnect; and

an interconnect of a second microelectronic die substrate electrically and directly coupled to the interconnect material.

27. (Previously presented) The semiconductor device of claim 26, wherein said electrically conductive reflowable material is lead solder or lead-free solder.

28. (Previously presented) A semiconductor device, comprising:

a carrier substrate having a bond pad;

a first microelectronic die substrate, the first microelectronic die substrate including,

an active side and a back side,

an active side interconnect, the active side interconnect disposed on the active side, coupled to the bond pad of the carrier substrate,

a backside interconnect disposed on the back side, coupled to and in substantial vertical alignment with the active side interconnect,

a redistributed interconnect of the backside interconnect, disposed on the backside, coupled to and offset from the backside interconnect;

an interconnect material consisting an electrically conductive adhesive, the interconnect material being coupled directly with the redistributed interconnect; and

an interconnect of a second microelectronic die substrate electrically and directly coupled to the interconnect material.

29. (Previously presented) The semiconductor device of claim 27, wherein said interconnect material is silver-loaded epoxy.

EVIDENCE APPENDIX

- None -

RELATED PROCEEDINGS APPENDIX

- None -